

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2000-124310

(43)Date of publication of application : 28.04.2000

(51)Int.Cl.

H01L 21/768  
H01L 21/28  
H01L 21/3205

(21)Application number : 10-294955

(71)Applicant : MATSUSHITA ELECTRONICS  
INDUSTRY CORP

(22)Date of filing : 16.10.1998

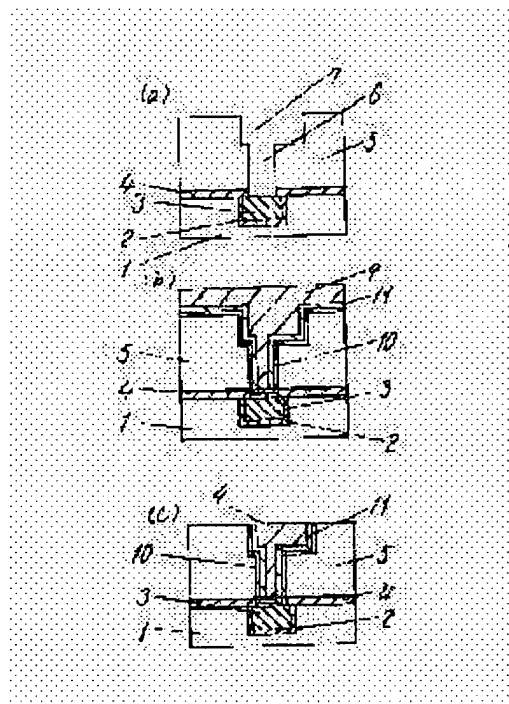
(72)Inventor : SEKIGUCHI MITSURU  
YAMADA TATSUYA

## (54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

### (57)Abstract:

PROBLEM TO BE SOLVED: To improve the (111) orientation of Cu and the electromigration resistance of an upper layer wiring by setting to a specified atm.% the nitrogen content of a tantalum nitride film adjacent to a Cu film constituting wirings.

SOLUTION: In a first insulation film 1 a barrier metal (tantalum nitride film) 2 and a first wiring of a first Cu film 3 are formed, the first Cu film 3 is covered with a silicon nitride film 4 and a second insulation film 5, contact holes 6 and wiring trenches 7 are formed into the second insulation film 5, a Ta film 10 is formed in the contact holes 6 and wiring trenches 7, a TaNx film 11 contg. 1-35 atm.% nitrogen is formed thereon, and a second Cu film 9 is deposited thereon so as to bury the contact holes 6 and wiring trenches 7. A part of a lower wiring adjacent to the first Cu film 3 has a nitrogen content of 1-0% and hence can hold the contact resistance lowered by 30%, the TaNx film 11 contg. 1-35 atm.% nitrogen is used beneath an upper layer wiring and the (111) orientation of Cu can be improved.



## LEGAL STATUS

[Date of request for examination] 13.06.2003

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than withdrawal the examiner's decision of rejection or application converted registration]

[Date of final disposal for application] 25.03.2004

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

## \* NOTICES \*

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

## CLAIMS

---

### [Claim(s)]

[Claim 1] The nitrogen content of said tantalum night RAIDO film of the part which it is the semiconductor device equipped with wiring which uses copper as a principal component, and the copper film which constitutes said wiring is in contact with the tantalum night RAIDO film, and touches said copper film is the semiconductor device made into 1 - 35% by atomic %.

[Claim 2] The nitrogen content of the tantalum night RAIDO film of the part which it is the semiconductor device equipped with the upper wiring and lower layer wiring which use copper as a principal component, and the nitrogen content of the tantalum night RAIDO film of the part which each of said upper wiring and said lower layer wiring touches the tantalum night RAIDO film, and touches said upper wiring is 1 - 35% in atomic %, and touches said lower layer wiring is a semiconductor device which is 1% or less of the tantalum night RAIDO film or the tantalum film.

[Claim 3] It is the semiconductor device equipped with the upper wiring and lower layer wiring which use copper as a principal component. The nitrogen content of the tantalum night RAIDO film of the part which each of said upper wiring and said lower layer wiring touches the tantalum night RAIDO film, and touches said upper wiring The nitrogen content of the tantalum night RAIDO film of the part which is 1 - 35% in atomic %, and touches said lower layer wiring is a semiconductor device which is 35 - 50% of tantalum night RAIDO film, or the tantalum film in atomic %.

[Claim 4] The nitrogen content of the tantalum night RAIDO film of the part which touches the upper wiring is a semiconductor device according to claim 2 which is increasing the nitrogen content continuously according to the thickness which goes in said upper wiring direction.

[Claim 5] The nitrogen content of the tantalum night RAIDO film of the part which touches lower layer wiring is a semiconductor device according to claim 3 which are decreasing in number the nitrogen content continuously according to the thickness which goes in said lower layer wiring direction.

[Claim 6] The process which forms an insulator layer on the 1st copper wiring, and forms the contact hole which said 1st copper wiring exposed into said insulator layer, and the wiring gutter for the 2nd wiring, The process which forms in said contact hole and said wiring Mizogami the tantalum film or the 1st film whose nitrogen content is the tantalum night RAIDO film below 1 atom %, The process which forms the 2nd film whose nitrogen content is 1 - 35% of tantalum night RAIDO film in atomic % on said 1st film, The process which deposits the film which serves as the 2nd copper wiring so that said contact hole and said wiring gutter may be embedded on said 2nd film, The manufacture approach of a semiconductor device of having the process which removes the film used as said 1st film other than said wiring gutter, the 2nd film, and the 2nd copper wiring, and forms the 2nd copper wiring.

[Claim 7] The process which forms an insulator layer on the 1st copper wiring, and forms the contact hole which said 1st copper wiring exposed into said insulator layer, and the wiring gutter for the 2nd wiring, The process which forms in said contact hole and said wiring Mizogami the 1st film whose nitrogen content is 35 - 50% of tantalum night RAIDO film in atomic %, The process which forms the 2nd film whose nitrogen content is 1 - 35% of tantalum night RAIDO film in atomic % on said 1st film, The process which deposits the film which serves as the 2nd copper wiring so that said contact hole and

said wiring gutter may be embedded on said 2nd film, The manufacture approach of a semiconductor device of having the process which removes the film used as said 1st film other than said wiring gutter, the 2nd film, and the 2nd copper wiring, and forms the 2nd copper wiring.

[Claim 8] The manufacture approach of a semiconductor device according to claim 6 of having the process which deposits the tantalum nitride RAIDO film which increased to 1 - 35% on the maximum front face in a contact hole and wiring Mizogami from 0 - 1% of the part to which a nitrogen content touches a lower layer copper film in the direction of thickness.

[Claim 9] The manufacture approach of a semiconductor device according to claim 7 of having the process which deposits the tantalum nitride RAIDO film which decreased in number to 1 - 35% on the maximum front face from 35 - 50% of the part to which a nitrogen content touches a contact hole and wiring Mizogami with a lower layer copper film in the direction of thickness.

[Claim 10] It is the manufacture approach of the semiconductor device according to claim 8 to which make the partial pressure of N<sub>2</sub> gas into 0 - 40% at the film deposition beginning, and it is made to change continuously with 40 - 57% at the time of film deposition termination in case it forms by the reactant spatter using Ta target and Ar+N<sub>2</sub> mixed gas as an approach of forming the tantalum nitride RAIDO film to which the nitrogen content was made to increase in the direction of thickness.

[Claim 11] It is the manufacture approach of the semiconductor device according to claim 9 to which make the partial pressure of N<sub>2</sub> gas into 57 - 67% at the film deposition beginning, and it is made to change continuously with 40 - 57% at the time of film deposition termination in case it forms by the reactant spatter using Ta target and Ar+N<sub>2</sub> mixed gas as an approach of forming the tantalum nitride RAIDO film which decreased the nitrogen content in the direction of thickness.

---

[Translation done.]

\* NOTICES \*

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

## DETAILED DESCRIPTION

---

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the semiconductor device equipped with copper wiring which has the tantalum nitride RAIDO film, and its manufacture approach.

[0002]

[Description of the Prior Art] since it became impossible to disregard delay by CR component of wiring to improvement in the speed of a transistor in the silicon LSI after 0.18-micrometer generation -- the conventional aluminum wiring (3micro ohm-cm of specific resistance) -- changing -- more -- low -- resistance (1.7micro ohm-cm of specific resistance) -- examination which uses copper for a wiring material is progressing. Moreover, the current density passed to wiring with detailed-izing of a component is increasing for every generation, and needs to raise the resistance also to the phenomenon of the electromigration which a wiring material is pushed on an electron, moves at the time of current impression, and wiring disconnects. It is expected that it will be expected that deformation, i.e., migration of an atom, cannot take place easily since the melting point is high compared with aluminum, and the copper of electromigration resistance will also be expensive.

[0003] However, there is a report [Y. Igarashi et al, VLSI Symp., p.76, and 1996] that electromigration resistance gets worse, and it is necessary to improve electromigration resistance also in copper wiring by detailed wiring about 0.3-micrometer width of face, also in copper wiring.

[0004] In copper wiring, copper is spread in an insulator layer by heat treatment of about 400 degrees C in a wiring process, and since it is necessary to prevent leak between wiring increasing, it is necessary to prepare the barrier film which prevents copper diffusion between a copper film and an insulator layer. Promising \*\* of the tantalum nitride RAIDO film with the barrier property strong as barrier film to copper diffusion is carried out most.

[0005] Hereafter, the copper wiring technique using the tantalum nitride RAIDO film is explained using drawing 5 (for example, IITC besides M. Moussavi, p.295, 1998).

[0006] First, slot wiring which consists of barrier metal 2 and the 1st copper film 3 is formed into the 1st insulator layer 1 on a semiconductor device like drawing 5 (a), and a contact hole 6 and a wiring gutter 7 are formed in the semiconductor device covered by the silicon nitride 4 and the 2nd insulator layer 5. Here, the barrier metal 2 and the silicon nitride 4 have played the role which prevents spreading copper in an insulator layer by heat treatment of about 400 degrees C in a wiring process. The tantalum nitride RAIDO film is sufficient as the barrier metal 2. Next, the TaNx (tantalum nitride RAIDO) film 8 is deposited in the reactant spatter using Ta target and Ar+N2 mixed gas like drawing 5 (b).

[0007] Next, after depositing the copper film which serves as a conductive layer by the spatter, a copper film is deposited with electrolysis plating, the 2nd copper film 9 is formed, and a contact hole 6 and a wiring gutter 7 are embedded. Next, like drawing 5 (c), by the CMP method etc., the TaNx film 8 of the wiring gutter exterior and the 2nd copper film 9 are removed, and wiring is formed. A silicon nitride and an insulator layer are deposited, the process after drawing 5 (a) is repeated, and a multilayer interconnection is formed by the back.

[0008] Here, about the TaNx film, that contact resistance with the 1st copper film which constitutes lower layer wiring is low, that the barrier property to diffusion into a copper insulator layer is high, and raising the dependability of the upper wiring it is unreliable from the 2nd copper film are expected.

[0009]

[Problem(s) to be Solved by the Invention] it is known that barrier property will become high, so that the content of nitrogen is high -- \*\*\*\* (J.Vac.Sci.Tech.B 14 besides Takeyama, p.674, 1996) -- the optimum value of a nitrogen content exerted on the dependability of contact resistance and wiring is not reported until now.

[0010] This invention is mainly deciding the optimum value of the content of the nitrogen in the TaNx film, is still more reliable than copper wiring considered for semiconductor devices until now, and offers the semiconductor device which has low contact resistance and copper wiring of high barrier property, and its manufacture approach.

[0011]

[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device of this invention makes the nitrogen content of the tantalum night RAIDO film part which touches the copper film of the upper wiring 1 - 35% by atomic %.

[0012] Moreover, the semiconductor device of this invention is considered as the configuration used as the tantalum film, or it makes into 1 - 35% the nitrogen content of the tantalum night RAIDO film part which touches the copper film of the upper wiring by atomic % and a nitrogen content uses as 1% or less of tantalum night RAIDO film the tantalum night RAIDO film part which touches the copper film of lower layer wiring.

[0013] Moreover, the semiconductor device of this invention is considered as the configuration which made the nitrogen content of the tantalum night RAIDO film part which touches the copper film of the upper wiring 1 - 35% by atomic %, and made the nitrogen content of the tantalum night RAIDO film part which touches the copper film and insulator layer of lower layer wiring 35 - 50%.

[0014] Moreover, the semiconductor device of this invention makes the nitrogen content of the tantalum night RAIDO film part which touches the copper film of lower layer wiring 0 - 1% by atomic %, makes a nitrogen content increase in the direction of thickness continuously, and is considered as the configuration which made the nitrogen content of the tantalum night RAIDO film part which touches a copper film 1 - 35% by atomic %.

[0015] Moreover, the semiconductor device of this invention makes the nitrogen content of the tantalum night RAIDO film part which touches the copper film of lower layer wiring 35 - 50% by atomic %, decreases a nitrogen content continuously in the direction of thickness, and considers it as the configuration which made the nitrogen content of the tantalum night RAIDO film part which touches a copper film 1 - 35% by atomic %.

[0016] Moreover, it is characterized by the contact hole where the 1st copper film exposed the manufacture approach of the semiconductor device of this invention, the process at which the tantalum film or a nitrogen content forms 1% or less of tantalum night RAIDO film in wiring Mizogami, and said tantalum film or nitrogen content having the process from which a nitrogen content forms 1 - 35% of tantalum night RAIDO film by atomic % on 1% or less of tantalum night RAIDO film.

[0017] Moreover, the manufacture approach of the semiconductor device of this invention is characterized by having the contact hole which the 1st copper film exposed, the process from which a nitrogen content forms 35 - 50% of tantalum night RAIDO film in wiring Mizogami by atomic %, and the process which forms the tantalum night RAIDO film whose nitrogen content is 1 - 35% on the tantalum night RAIDO film said whose nitrogen content is 35 - 50%.

[0018] Moreover, the manufacture approach of the semiconductor device of this invention is characterized by having the process which deposits the tantalum night RAIDO film which the nitrogen content began from 0 - 1% in the direction of thickness, and increased to the contact hole and wiring Mizogami whom the 1st copper film exposed to 1 - 35% on the maximum front face.

[0019] Moreover, the manufacture approach of the semiconductor device of this invention is characterized by having the process which deposits the tantalum night RAIDO film which the nitrogen

content began from 35 - 50% in the direction of thickness, and decreased in number to 1 - 35% on the maximum front face to the contact hole and wiring Mizogami whom the 1st copper film exposed.

[0020] Moreover, in case the manufacture approach of the semiconductor device of this invention is formed by the reactant spatter using Ta target and Ar+N<sub>2</sub> mixed gas as an approach of forming the tantalum nitride RAIDO film to which the nitrogen content was made to increase in the direction of thickness, it makes the partial pressure of N<sub>2</sub> gas 0 - 40% at the film deposition beginning, and it is characterized by making it change continuously with 40 - 57% at the time of film deposition termination.

[0021] Moreover, in case the manufacture approach of the semiconductor device of this invention is formed by the reactant spatter using Ta target and Ar+N<sub>2</sub> mixed gas as an approach of forming the tantalum nitride RAIDO film to which the nitrogen content was made to increase in the direction of thickness, it makes the partial pressure of N<sub>2</sub> gas 57 - 67% at the film deposition beginning, and it is characterized by making it change continuously with 40 - 57% at the time of film deposition termination.

[0022]

[Embodiment of the Invention] (1st operation gestalt) The semiconductor device of this invention is explained. In this operation gestalt, film with which a nitrogen content becomes 1 - 35% to the TaN<sub>x</sub> film 8 in the conventional technique is used. Other processes are as the Prior art having explained.

[0023] Hereafter, the cause whose electromigration resistance of the 2nd-layer wiring improves according to this operation gestalt is described.

[0024] The measurement result of the copper (111) reinforcement by the nitrogen content of the TaN<sub>x</sub> film and the X-ray diffraction method of the sample which deposited 50nm thickness for the copper film in the spatter on condition that a room temperature and 2mTorr on it was summarized to drawing 6.

Moreover, the measurement result of the contact resistance to lower layer copper wiring was also doubled and described. After sample conditions performed Ar spatter in the diameter kelvin contact with a depth of 300nm of 0.35 micrometer by oxide film etching 25nm, they deposited 25nm of TaN<sub>x</sub> film with which nitrogen contents differ, deposited 500nm of copper for copper after 100nm deposition and with electrolysis plating, and embedded and formed the contact hole and the wiring gutter. Measured value shows the average of 52 points, and standard deviation in the wafer side. According to this, it turns out that the copper stacking tendency (111) of a nitrogen content improves rather than Ta film top at 1 - 35%. This is considered to be because for the TaN<sub>x</sub> film 8 to have changed into the amorphous condition that the microcrystal which is Ta<sub>2</sub>N is included and for copper wettability to have improved as shown in drawing 4. In the dependability of copper wiring, on Ta, since a copper (111) stacking tendency improves, it is reported that electromigration resistance improves (201 Proc. besides C.Ryu IRPS., p. 1997).

[0025] In this experiment, on the TaN<sub>x</sub> film 8 whose nitrogen content is 1 - 35%, since a copper stacking tendency (111) improves rather than Ta top, it is expected that the dependability of copper wiring can improve.

[0026] On the other hand, it is thought that copper (111) reinforcement is lower than Ta top at 35 - 50%, and the dependability of copper wiring falls [ a nitrogen content ] rather than Ta top. Moreover, at 50% or more, the specific resistance of the TaN<sub>x</sub> film becomes more than 2100micro ohm-cm, and it also turns out that the contact resistance to lower layer copper wiring increases. Therefore, the improvement in dependability of copper wiring is expected on the TaN<sub>x</sub> film 8 whose nitrogen content is 1 - 35%. Therefore, according to this invention, by restricting the nitrogen content in the TaN<sub>x</sub> film 8 to 1 - 35%, the semiconductor device which has copper wiring with high electromigration resistance is obtained.

[0027] (2nd operation gestalt) Drawing 1 (a) - (c) is the operation gestalt of the copper wiring and the manufacture approach of a semiconductor device. First, slot wiring (1st wiring) with which it consists of barrier metal 2 and the 1st copper film 3 is formed into the 1st insulator layer (silicon oxide) 1 by which the process of drawing 1 (a) was formed on the silicon substrate. This wiring 3 is covered by the silicon nitride 4 and the 2nd insulator layer 5. A contact hole 6 and a wiring gutter 7 are formed in the 2nd insulator layer 5. Here, the barrier metal 2 and the silicon nitride 4 have played the role which prevents

spreading copper in an insulator layer by heat treatment of about 400 degrees C in a wiring process. The tantalum nitride RAIDO film is sufficient as the barrier metal 2.

[0028] Next, like drawing 1 (b), the Ta film 10 is formed in a contact hole and a wiring gutter, and 1 - 35% of TaN<sub>x</sub> film 11 is formed for a nitrogen content by atomic % on it. The 2nd copper film 9 is deposited with electrolysis plating etc. so that a contact hole and a wiring gutter may be embedded on it.

[0029] In drawing 1 (c), the 2nd copper film 9, the TaN<sub>x</sub> film 11, and the Ta film 10 are removed by the CMP method etc., and wiring is formed.

[0030] Since the part which is in contact with the 1st copper film of lower wiring is film whose nitrogen content is 1 - 0% according to this invention, as shown also in drawing 6, contact resistance can maintain the value low about 30 percent at the time of using the film whose nitrogen content is 1 - 35%. Moreover, since the TaN<sub>x</sub> film whose nitrogen content is 1 - 35% is used for the bottom of the upper copper wiring, its copper stacking tendency (111) improves rather than the case where there is only the Ta film 10. Therefore, it is expected that the dependability of copper wiring will improve.

[0031] Thus, in this invention, the contact resistance to lower layer wiring can be lowered, and the dependability of the upper wiring can be raised.

[0032] (3rd operation gestalt) Drawing 2 (a) - (c) is the operation gestalt of copper wiring for semiconductor devices, and its manufacture approach. First, in the semiconductor device with which slot wiring with which it consists of barrier metal 2 and the 1st copper film 3 is formed into the 1st insulator layer 1 on a semiconductor device, and the process of drawing 2 (a) is covered by the silicon nitride 4 and the 2nd insulator layer 5, a contact hole 6 and a wiring gutter 7 are formed. Here, the barrier metal 2 and the silicon nitride 4 have played the role which prevents spreading copper in an insulator layer by heat treatment of about 400 degrees C in a wiring process. The tantalum nitride RAIDO film is sufficient as the barrier metal 2.

[0033] Next, like drawing 2 (b), 35 - 50% of TaN<sub>x</sub> film 12 is formed for a nitrogen content by atomic %, and 1 - 35% of TaN<sub>x</sub> film 11 is formed for a nitrogen content by atomic % on it. The 2nd copper film 9 is deposited with electrolysis plating etc. so that a contact hole and a wiring gutter may be embedded on it.

[0034] In drawing 2 (c), the 2nd copper film 9, the TaN<sub>x</sub> film 11, and the TaN<sub>x</sub> film 12 are removed by the CMP method etc., and wiring is formed.

[0035] According to this invention, since a nitrogen content is the TaN<sub>x</sub> film 12 which is 35 - 50%, even if the part which is in contact with the 2nd insulator layer has high barrier property and uses higher heat treatment temperature at a wiring process, it has the advantage that copper diffusion can be controlled. However, in order to make it considering contact resistance with lower layer wiring not exceed 10 ohms with the diameter of 0.35 micrometer as shown also in drawing 6, it is necessary to make a nitrogen content 50% or less.

[0036] Moreover, by this invention, since the TaN<sub>x</sub> film whose nitrogen content is 1 - 35% is used for the bottom of the upper copper wiring, the copper stacking tendency (111) of a nitrogen content improves by atomic % rather than the case on 35 - 50% of TaN<sub>x</sub> film. Therefore, it is expected that the dependability of copper wiring will improve. Thus, in this invention, the semiconductor device which raised the barrier property to diffusion into a copper insulator layer, and raised the dependability of the upper wiring can be obtained.

[0037] (4th operation gestalt) Drawing 3 (a) - (c) is the operation gestalt of the copper wiring for semiconductor devices and the manufacture approach given in claims 4, 8, and 10. In the semiconductor device with which slot wiring with which it consists of barrier metal 2 and the 1st copper film 3 is formed into the 1st insulator layer 1 on a semiconductor device, and the process of this drawing 3 (a) is covered by the silicon nitride 4 and the 2nd insulator layer 5, a contact hole 6 and a wiring gutter 7 are formed. Here, the barrier metal 2 and the silicon nitride 4 have played the role which prevents spreading copper in an insulator layer by heat treatment of about 400 degrees C in a wiring process. The tantalum nitride RAIDO film is sufficient as the barrier metal 2.

[0038] Next, the TaN<sub>x</sub> film 13 with which nitrogen contents differ in the direction of thickness is formed by making it change continuously with 40 - 57% by the reactant spatter using Ta target and



Ar+N<sub>2</sub> mixed gas like drawing 3 (b) at the time of film deposition termination by making the partial pressure of N<sub>2</sub> gas into 0 - 40% at the film deposition beginning. On the indicated conditions, reference of drawing 6 obtains the TaN<sub>x</sub> film 13 whose nitrogen content of the part to which the nitrogen content of the part which touches the copper film of lower layer wiring touches the copper film of the upper wiring at 0 - 1% is 1 - 35%.

[0039] Next, the 2nd copper film 9 is deposited with electrolysis plating etc. so that a contact hole and a wiring gutter may be embedded on it.

[0040] In drawing 3 (c), the 2nd copper film 9 and the TaN<sub>x</sub> film 13 are removed by the CMP method etc., and wiring is formed.

[0041] In this invention, since a nitrogen content is the film which is 1 - 0%, the part which is in contact with the 1st copper film of lower wiring can maintain the contact resistance low about 30 percent at the time of using the film whose nitrogen content is 1 - 35%, as shown also in drawing 6. Moreover, since the TaN<sub>x</sub> film whose nitrogen content is 1 - 35% is used, it is expected by the bottom of the upper copper wiring that the dependability of copper wiring will improve. Thus, in this invention, like the 2nd operation gestalt, the contact resistance to lower layer wiring can be lowered, and the dependability of the upper wiring can be raised. changing continuously the partial pressure of the nitrogen at the time of a reactant spatter by this invention furthermore -- the TaN<sub>x</sub> film 13 -- the role of both the TaN<sub>x</sub> film 11 in the 2nd operation gestalt and the Ta film 10 can be played in one layer, and there is also an advantage that a process becomes simple.

[0042] (5th operation gestalt) Drawing 3 (a) The operation gestalt of copper wiring for semiconductor devices and its manufacture approach is also explained using - (c). In the semiconductor device with which slot wiring with which it consists of barrier metal 2 and the 1st copper film 3 is formed into the 1st insulator layer 1 on a semiconductor device, and the process of drawing 3 (a) is covered by the silicon nitride 4 and the 2nd insulator layer 5, a contact hole 6 and a wiring gutter 7 are formed. Here, the barrier metal 2 and the silicon nitride 4 have played the role which prevents spreading copper in an insulator layer by heat treatment of about 400 degrees C in a wiring process. The tantalum nitride RAIDO film is sufficient as the barrier metal 2.

[0043] Next, the TaN<sub>x</sub> film 13 with which nitrogen contents differ in the direction of thickness is formed by making it change continuously with 40 - 57% by the reactant spatter using Ta target and Ar+N<sub>2</sub> mixed gas like drawing 3 (b) at the time of film deposition termination by making the partial pressure of N<sub>2</sub> gas into 57 - 67% at the film deposition beginning. On the indicated conditions, reference of drawing 6 obtains the TaN<sub>x</sub> film 11 whose nitrogen content of the part to which the nitrogen content of the part which touches the copper film of lower layer wiring touches the copper film of the upper wiring at 35 - 50% is 1 - 35%. Next, the 2nd copper film 9 is deposited with electrolysis plating etc. so that a contact hole and a wiring gutter may be embedded on it. In drawing 3 (c), the 2nd copper film 9 and the TaN<sub>x</sub> film 13 are removed by the CMP method etc., and wiring is formed.

[0044] In this invention, since a nitrogen content is the TaN<sub>x</sub> film which is 35 - 50%, even if the part which is in contact with the 2nd insulator layer has high barrier property and uses higher heat treatment temperature at a wiring process, it has the advantage that copper diffusion can be controlled. However, considering contact resistance with lower layer wiring, as shown also in drawing 6, it is necessary to make a nitrogen content 50% or less for making it not exceed 10 ohms with the diameter of 0.35 micrometer.

[0045] Moreover, in this invention, since the TaN<sub>x</sub> film whose nitrogen content is 1 - 35% is used and the copper stacking tendency (111) of a nitrogen content improves by atomic % rather than the case on 35 - 50% of TaN<sub>x</sub> film, it is expected by the bottom of the upper copper wiring that the dependability of copper wiring will improve. Thus, in this invention, the semiconductor device which raised the barrier property to an insulator layer and raised the dependability of the upper wiring can be obtained.

[0046] changing continuously the partial pressure of the nitrogen at the time of a reactant spatter by this invention furthermore -- the TaN<sub>x</sub> film 13 -- the role of both the TaN<sub>x</sub> film 11 in the 2nd operation gestalt and the Ta film 10 can be played in one layer, and there is also an advantage that a process becomes simple.

[0047] In the above operation gestalten 1-5, although the 1st copper film 3 and the 2nd copper film 9 used the pure copper, other copper alloys may be formed. Moreover, the alloy containing other metals [ copper ] with low contact resistance, for example, Ti etc., a compound with such Si, B, C, and N, or these etc. may be used for a change of the Ta film 10. If the embedding of the copper film 9 to a wiring gutter is possible, it may use the approaches of a throat, such as the electrolysis plating, CVD method, CVD+ elevated-temperature spatter, and spatter + reflow method and the ion plating method.

[0048] Moreover, the 1st and 2nd insulator layer does not need to be a silicon nitride, and may use the CVD film with the low dielectric constant containing the spreading film, SiO<sub>2</sub> film, or C. Moreover, although the approach of embedding a contact hole and a wiring gutter as wiring structure at coincidence was used, you may also embed either by this approach. Moreover, this invention may be applied not to slot wiring but to wiring using copper dry etching.

[0049]

[Effect of the Invention] The semiconductor device of this invention can improve the electromigration resistance of the upper wiring by making into 1 - 35% the nitrogen content of the tantalum nitride RAIDO film part which touches the copper film of the upper wiring by atomic %, and raising a copper (111) stacking tendency.

[0050] In this invention, the nitrogen content of the tantalum nitride RAIDO film part which touches the copper film of the upper wiring is made into 1 - 35% by atomic %, and the electromigration resistance of the upper wiring can be secured. Moreover, or a nitrogen content uses as 1% or less of tantalum nitride RAIDO film the tantalum nitride RAIDO film part which touches the copper film of lower layer wiring, by considering as the tantalum film, penetration of the nitrogen to the lower layer wiring section can be pressed down, and contact resistance can be pressed down low.

[0051] In this invention, the nitrogen content of the tantalum nitride RAIDO film part which touches the copper film of the upper wiring is made into 1 - 35% by atomic %, and the electromigration resistance of the upper wiring can be secured. Moreover, the barrier property to copper can be strengthened with making into 35 - 50% the nitrogen content of the tantalum nitride RAIDO film part which touches the copper film and insulator layer of lower layer wiring, and the upper limit of the heat treatment temperature in the inside of a wiring process can be raised by it.

[0052] The semiconductor device of this invention makes the nitrogen content of the tantalum nitride RAIDO film part which touches the copper film of lower layer wiring 0 - 1% by atomic %, makes a nitrogen content increase in the direction of thickness continuously, and is characterized by making into 1 - 35% the nitrogen content of the tantalum nitride RAIDO film part which touches a copper film by atomic %. In one layer of tantalum nitride RAIDO layers, electromigration resistance of the upper wiring can be made high, and contact resistance with the lower layer wiring section can be pressed down low.

[0053] In this invention, the nitrogen content of the tantalum nitride RAIDO film part which touches the copper film of lower layer wiring is made into 35 - 50% by atomic %, and a nitrogen content is continuously decreased in the direction of thickness, and it is characterized by making into 1 - 35% the nitrogen content of the tantalum nitride RAIDO film part which touches a copper film by atomic %. In one layer of tantalum nitride RAIDO layers, electromigration resistance of the upper wiring can be made high, and diffusion into a copper insulator layer can also be pressed down.

[0054] As mentioned above, according to this invention, copper wiring with low contact resistance with lower layer wiring with the high and electromigration resistance of the upper wiring is obtained by controlling the nitrogen content of the tantalum nitride RAIDO film which touches a copper film. Moreover, according to another claim, copper wiring whose electromigration resistance of the upper wiring can also press down diffusion into a copper insulator layer highly is obtained by controlling the nitrogen content of the tantalum nitride RAIDO film which touches a copper film.

---

[Translation done.]

**\* NOTICES \***

JPO and NCIPi are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

---

**DESCRIPTION OF DRAWINGS**

---

[Brief Description of the Drawings]

[Drawing 1] The sectional view showing the manufacture approach of copper wiring for semiconductor devices in the 2nd operation gestalt

[Drawing 2] The sectional view showing the manufacture approach of copper wiring for semiconductor devices in the 3rd operation gestalt

[Drawing 3] The sectional view showing the manufacture approach of copper wiring for semiconductor devices in the operation gestalt of the 4th and 5

[Drawing 4] Drawing showing the crystallinity of the TaNx film

[Drawing 5] The sectional view showing the manufacture approach of copper wiring of the conventional semiconductor device

[Drawing 6] Drawing showing the stacking tendency of the membraneous quality of the TaNX film, and the copper of copper wiring, and the relation of contact resistance

[Description of Notations]

1 1st Insulator Layer

2 Barrier Metal

3 1st Copper Film

4 Silicon Nitride

5 2nd Insulator Layer

6 Contact Hole

7 Wiring Gutter

8 TaNx Film

9 2nd Copper Film

10 Ta Film

11 TaNx Film Which Contains N 1 to 35%

12 TaNx Film Which Contains N 35 to 50%

13 TaNx Film with which N Contents Differ in the Direction of Thickness

---

[Translation done.]

## \* NOTICES \*

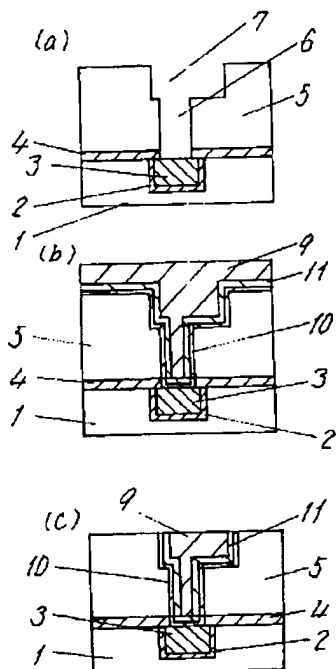
JPO and NCIPi are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. \*\*\*\* shows the word which can not be translated.
3. In the drawings, any words are not translated.

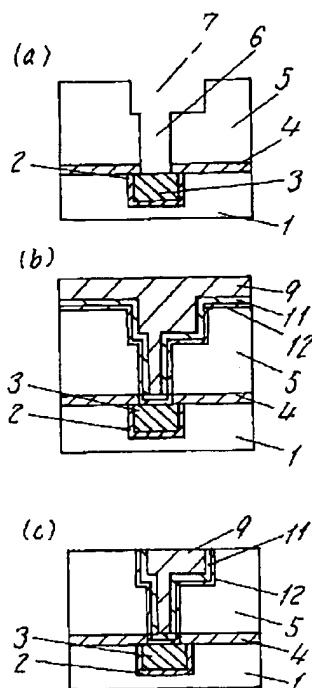
## DRAWINGS

[Drawing 1]

- |           |  |
|-----------|--|
| 1 第1の絶縁膜  | 6 コンタクトホール   |
| 2 バリヤメタル  | 7 配線溝  |
| 3 第1のCu膜  | 9 第2のCu膜   |
| 4 シリコン窒化膜 | 10 Ta膜   |
| 5 第2の絶縁膜  | 11 N <sub>2</sub> /35%含む<br>Ta <sub>2</sub> N <sub>5</sub> 膜 |

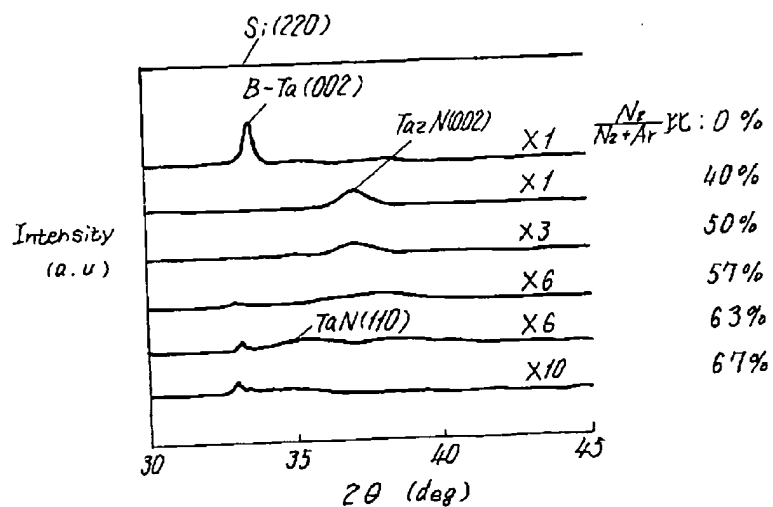
[Drawing 2]

- |           |                         |
|-----------|-------------------------|
| 1 第1の絶縁膜  | 6 コンタクトホール              |
| 2 バリアメタル  | 7 配線溝                   |
| 3 第1のCu膜  | 9 第2のCu膜                |
| 4 シリコン窒化膜 | 11 Nを1~35%含む<br>Ta/Nx膜  |
| 5 第2の絶縁膜  | 12 Nを35~50%含む<br>Ta/Nx膜 |



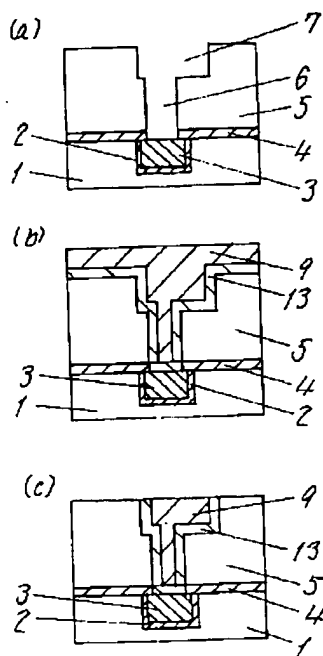
[Drawing 4]

Ta/Nx膜結晶性のXRDスペクトル (N<sub>2</sub>分圧依存性)



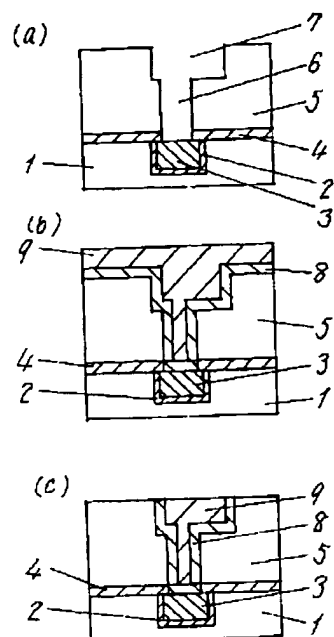
[Drawing 3]

- |           |                       |
|-----------|-----------------------|
| 1 第1の絶縁膜  | 6 コンタクトホール            |
| 2 バリウム    | 7 配線溝                 |
| 3 第1のCu膜  | 9 第2のCu膜              |
| 4 シリコン窒化膜 | 13 N含有量が膜厚方向に異なるTaNx膜 |
| 5 第2の絶縁膜  |                       |



[Drawing 5]

- 1 第1の絶縁膜    6 コンタクトホール  
 2 バリメタル    7 配線溝  
 3 第1のCu膜    8 TaNx膜  
 4 シリコン窒化膜    9 第2のCu膜  
 5 第2の絶縁膜



[Drawing 6]

TaNx膜の膜質とCu(111)配向性・コンタクト抵抗の関係

膜厚数	Ta	TaNx	TaNx	TaNx	TaNx	TaNx
成膜時のN <sub>2</sub> /(Ar+N <sub>2</sub> )比(%)	0	20	50	37	63	67
RBS分析による膜中N含有量(%)	0	1	20	35	43	50
TaNx上Cu(111)回折強度	16500	24000	29700	15000	5300	4500
膜比抵抗(mΩcm)	170	150	220	220	600	2100
0.35μm径コンタクト抵抗(Ω)	平均値	0.59	0.81	0.88	1.14	2.51
	標準偏差	0.15	0.15	0.16	0.28	0.86
						8

[Translation done.]



US006376370B1

(12) **United States Patent**  
**Farrar**

(10) **Patent No.: US 6,376,370 B1**  
(45) **Date of Patent: Apr. 23, 2002**

(54) **PROCESS FOR PROVIDING SEED LAYERS FOR USING ALUMINUM, COPPER, GOLD AND SILVER METALLURGY PROCESS FOR PROVIDING SEED LAYERS FOR USING ALUMINUM, COPPER, GOLD AND SILVER METALLURGY**

(75) **Inventor: Paul A. Farrar, So. Burlington, VT (US)**

(73) **Assignee: Micron Technology, Inc., Boise, ID (US)**

(\*) **Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.**

(21) **Appl. No.: 09/484,002**

(22) **Filed: Jan. 18, 2000**

(51) **Int. Cl.<sup>7</sup> ..... H01L 21/44**

(52) **U.S. Cl. .... 438/678; 257/762**

(58) **Field of Search ..... 438/678, 608, 438/625, 642, 650, 652, 635; 437/189; 427/97; 257/762**

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

2,842,438 A	7/1958	Saarivirta et al. ....	75/153
4,762,728 A	8/1988	Keyser et al. ....	427/38
4,847,111 A	7/1989	Chow et al. ....	427/38
4,962,058 A	10/1990	Cronin et al. ....	437/187
5,084,412 A *	1/1992	Nakasaka ....	437/189

(List continued on next page.)

**FOREIGN PATENT DOCUMENTS**

JP 07078815 3/1995 ..... H01L/21/3205

**OTHER PUBLICATIONS**

Meng Hsiung Kiang, Michael A. Lieberman, Nathan W. Chung and X.Y.Qian, Appl. Phys.Lett.60 (22), Jun. 1, 1992, Pages. 2767-2769.\*

Shacham-Diamand, Y., et al., "Copper electroless deposition technology for ultra-large-scale-intergration (ULSI) metallization", *Microelectronic Engineering*, NL, vol. 33, No. 1, XP004054497, 47-58, (1997).

Stroud, P.T., et al., "Preferential deposition of silver induced by low energy gold ion implantation", *Thin Solid Films*, Switzerland, vol. 9, No. 2, XP000993098, 273-281, (Feb. 1972).

"Brooks Model 5964 High Performance Metal Seal Mass Flow Controller (Introduced in 1991)", *Brooks Instrument*, <http://www.frco.com/brooks/semiconductor/>

(List continued on next page.)

**Primary Examiner—David Nelms**

**Assistant Examiner—David Vu**

(74) **Attorney, Agent, or Firm—Schwegman, Lundberg, Woessner & Kluth, P.A.**

(57) **ABSTRACT**

Structures and methods are provided which improve performance in integrated circuits. The structures and methods include a diffusion barrier and a seed layer in an integrated circuit both formed using a low energy ion implantation followed by a selective deposition of metal lines for the integrated circuit. According to the teachings of the present invention, the selective deposition of the metal lines avoids the need for multiple chemical mechanical planarization (CMP) steps. The low energy ion implantation of the present invention allows for the distinct placement of both the diffusion barrier and the seed layer. A residual resist can be used to remove the diffusion barrier and the seed layer from unwanted areas on a wafer surface. The novel methodology of the present invention includes patterning an insulator material to define a number of trenches in the insulator layer opening to a number of first level vias in a planarized surface. A barrier/adhesion layer is deposited in the number of trenches using a low energy ion implantation, e.g. a 100 to 800 electron volt (e.v.) ion implantation. A seed layer is deposited on the barrier/adhesion layer in the number of trenches also using the low energy ion implantation. Structures formed by this novel process are similarly included within the scope of the present invention and account for aluminum, copper, gold, and silver metal interconnects.

**45 Claims, 47 Drawing Sheets**

